Extended Abstract: CNOT circuit synthesis for topologically-constrained quantum memories

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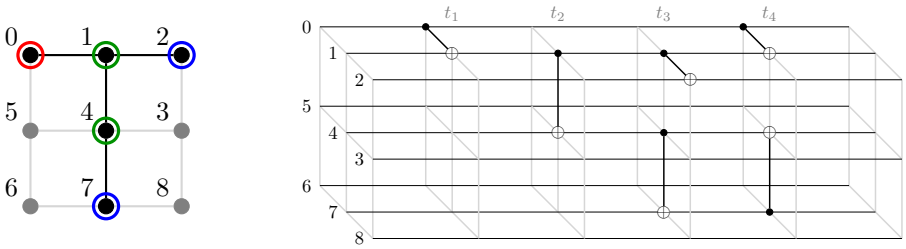
Executing quantum circuits on most current qunatum computers is constrained by the topology of the computer's qubits where two-qubit operations are typically only possible between pairs of systems that are adjacent in the 'coupling graph' of the architecture [9, 6, 10, 2, 1, 4, 5]. Naïvely, this can be addressed by simply inserting swap gates to move a pair of qubits next to each other before each 2-qubit operation. However, this approach comes with an enormous overhead in terms of 2-qubit operations which increases the circuit depth and total error. This approach only takes the topological structure of the circuit into account (i.e. which qubits are being acted upon) rather than semantic structure (i.e. the unitary being implemented), and hence miss out on opportunities for more efficient circuit mapping. In stead, one could re-synthesise the circuit from some representation of the unitary in a manner that is architecture aware.

We present a new approach to quantum circuit mapping, called STEINER-GAUSS, based on Gaussian elimination, and apply it in the simplest case of mapping CNOT circuits. We use a simple strategy for identifying and using appropriate intermediate rows based on *Steiner trees*. For our purposes, the set of vertices to build the Steiner tree over represents all of the rows that need to be reduced by primitive row operations (e.g. the rows containing non-zero entries below a pivot) whereas the tree itself gives us an efficient strategy for performing those reductions via nearest-neighbour CNOTs:



The end result is CNOT circuit realising a given parity map involving only nearest-neighbour interactions. In addition, we perform a simple genetic algorithm-based optimisation procedure, with a cost function given as the total resulting CNOT count, to find a good choice of initial qubit locations.

To measure the effectiveness of our approach, we produce many random CNOT circuits on 9, 16, and 20 qubits, containing between 3 and 256 CNOT gates, and map them onto 5 different graph topologies: 3×3 and 4×4 square lattices, 16-qubit architectures of the IBM QX-5 and Rigetti Aspen devices, and the 20-qubit IBM Q20 Tokyo architecture. To compare the performance of our technique to general-purpose mapping techniques, we also map these CNOT circuits with the Rigetti QuilC compiler and t|ket⟩ by Cambridge Quantum Computing. Using these as a baseline, we find an average savings in 2-qubit gates of 48% over QuilC and 36% over t|ket⟩.[3] These results can be found in the full paper.

Finally, we note that our algorithm has been improved since it first appeared in preprint [11, 3] as well as extended to circuits consisting of CNOTs and arbitrary Z-phase rotations [8, 7]. This shows that our algorithm marks the beginning of a new paradigm in quantum compiling. In our presentation, we will briefly survey these extensions and how they might be used in the future.

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[3]All circuits can be found in QASM format at: https://github.com/Quantomatic/pyzx/tree/steiner_decomp/circuits/steiner

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